REMARKS

Claims 2 to 7 are pending in the above-identified application. Claim 2 is independent.

Summary of the Present invention

The present invention is directed to a high-frequency multilayer circuit substrate used in a microwave band. The invention has as an objective to provide a multilayer circuit substrate capable of executing low-reflection low-loss inter-circuit-layer transmission with a simple structure and reduced manufacturing cost.

In an embodiment of the present invention, a plurality of circuit layers are connected to each other by a via hole, and the impedance of the via hole connecting portion matches the impedance of the signal transmission line, of the circuit layer connected by way of the via hole, by way of a planar impedance matching circuit forming a direct connection between the via hole and the signal transmission line. The via hole is provided with a via hole metal pad for connecting the via hole to the impedance matching circuit. Thus, matching the impedance of the via hole connecting portion to the impedance of the signal transmission line only requires adjusting the width and length of the impedance matching transmission line. Also, because of the direct connection of the impedance matching circuit to the transmission line of the circuit layer connected by the via hole, transmission loss is lowered.

Alternatively, an impedance matching portion is formed by the impedance matching transmission line and stubs connected to both sides of the transmission line at an end closest to the signal transmission line. The impedance is controlled by adjusting the width and length of the impedance matching transmission line and the width and length of each of the stubs.

In a further embodiment, an impedance matching circuit is formed by a plurality of planar impedance matching transmission lines having at least two different widths. The impedance is controlled by adjusting the widths and lengths of the impedance matching transmission lines.

Thus, Applicants have developed a structure having low manufacturing costs. Further, Applicants have determined that based on such a simple planar structure requiring only adjustment of the width and height of impedance matching transmission lines, a low transmission loss and a reduction in reflection loss can be achieved at a high frequency of about 60GHz (see Figures 5 and 10). Thus, the present invention is particularly suitable for millimeter band signal transmission.

Claim Rejections – 35 U.S.C. §102

Claims 2-3 have been rejected under 35 U.S.C. §102(b) as being clearly anticipated by Eda et al. (U.S. Patent 5,387,888, hereinafter Eda). Applicants respectfully traverse this rejection.

Claim 2 is directed to a high-frequency multilayer circuit substrate, which among other things includes a planar impedance matching circuit formed by an impedance matching transmission line, one end of which is connected to the via hole through a via hole metal pad and other end of which is directly connected to the signal transmission line, each of which is located on the same circuit layer. Applicants submit that Eda does not teach or suggest at least that claimed limitation.

> Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385 388 (Fed. Cir.); cert. Dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. Denied, 469 U.S. 851 (1984).

The Office Action presents an argument that Eda's impedance matching line 221 with one end connected to a via 224 and the other end connected to a transmission line 201 through a via 225 teaches the claimed planar impedance matching circuit. Applicants disagree at least for the reason that because Eda's impedance matching line connects to the transmission line through at least via 225, the characteristic impedance of the other via 224 and the impedance matching line 221 would not match the characteristic impedance of the transmission line 201. Rather, the impedance of the via 225 connecting the transmission line to the impedance matching line also must be taken into

account. Furthermore, the additional via 225 would lead to further signal wave reflection in the via (see present Specification, page 1, lines 11-16).

In any case, the claim has been amended to explicitly state that the planar impedance matching circuit has its other end directly connected to the signal transmission line, and that the planar impedance matching circuit and the signal transmission line are located on the same circuit layer. Accordingly, Applicants submit that Eda fails to teach at least this claimed element.

In addition, Eda does not disclose a via hole metal pad provided around the via hole. Such a metal pad facilitates connection of the via hole to the impedance matching transmission line, such that only the dimensions of the impedance matching transmission line need to be adjusted. Accordingly, for at least these reasons, Applicants respectfully request that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. §103

Claims 4 and 5 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Eda. Applicants respectfully traverse this rejection.

At least for the reasons above for claim 2, Applicants submit that Eda does not teach or suggest all claimed elements of claims 4 and 5, as well. Thus, at least for this reason the rejections fail to establish *prima facie* obviousness of claims 4 and 5. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claims 6 and 7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Eda in view of Okada et al. (U.S. Patent 5,701,128, hereinafter Okada). Applicants respectfully traverse this rejection.

At least for the same reason as above for claim 2, Applicants submit that all claimed elements are not taught or suggested for claims 6 and 7, as well. Furthermore, the Office Action relies on Okada for disclosing stubs connected to transmission lines is functionally equivalent to lines having different widths connected in series. Applicants submit that Okada does not make up for the deficiency in Eda of not teaching or suggesting an impedance matching line which connects a via hole to a signal transmission line. Accordingly, Applicants submit that at least for these additional reasons, the rejection fails to establish *prima facie* obviousness for claims 6 and 7. Applicants respectfully request that the rejection be withdrawn.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§1.17 and 1.136(a), Applicants respectfully petition for a two-month extension of time in which to file this reply. Attached is a check for the required fee of $410.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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